ABSTRACT

An assertion generating system is disclosed. In an assertion generating system 207, a graphical editor 201 generates design data of a semiconductor integrated circuit by graphically editing a specification (finite state machine, process sequence) of the semiconductor integrated circuit with the use of a state transition table and a state transition figure or by editing the process sequence into a timing chart and a time series figure based on user operations, and a syntax analyzer 203 and a property extractor 204 generate a property that verifies the specification of the semiconductor integrated circuit based on the design data. The assertion generator 205 converts the property into an assertion description language 206.